

## Temperature behavior of graphene conductance induced by piezoelectric effect in a ferroelectric substrate

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### Abstract

Graphene on a ferroelectric can be a promising candidate to create advanced field effect transistors, modulators and electrical transducers, providing that research of its electrotransport and electromechanical properties can be lifted up from empirical to analytical level. Recently we have shown that alternating "up" and "down" piezoelectric displacement of the ferroelectric domain surfaces can lead to the increase of graphene channel conductance at room temperature because of partial separation of the graphene channel from the ferroelectric substrate. The change of graphene conductance caused by piezoelectric effect requires systematic studies of ambient conditions impact on its manifestations. The theoretical work studies the temperature behavior of the graphene conductance changes induced by piezoelectric effect in a ferroelectric substrate with domain structure. We revealed the possibility of increasing up to 100 times the conductance of graphene channel on ferroelectric substrate by changing ambient temperature for a given gate voltage and channel length. Obtained results can open the way towards advanced applications of graphene on ferroelectric in piezo-resistive memories operating in a wide temperature range.

### I. INTRODUCTION

Since the time of the experimental discovery [1, 2] graphene and other 2D-semiconductors [3, 4, 5, 6, 7, 8, 9] are in the center of attention of researchers. The most recent works [7 - 9] open

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new possibilities of graphene making further fundamental and applied studies of its electrophysical and electromechanical properties highly relevant. Noteworthy the practical usage of graphene and other 2D-semiconductors critically depend on the optimal choice of electromechanical, electrophysical and physicochemical properties of the interfaces, substrates and gates [10]. In particular the choice of substrates with additional functionality degrees compatible with a given 2D-material is crucial [3, 11].

Since ferroelectric substrates possess the additional functionality related with their spontaneous polarization direction, graphene and other 2D semiconductors on ferroelectric substrates are promising candidates for research. A ferroelectric substrate can significantly affect the electronic properties of graphene [12, 13, 14, 15, 16], due to the low density of states of graphene at the Dirac point, which can be easily accessed by the high gating efficiency of the ferroelectric substrate [17, 18].

The direction of spontaneous polarization and the domain structure of the substrate can be controlled by an external electric field. The possibility is used in graphene field effect transistors (**GFETs**), where a single-layer graphene is a channel and an electric voltage applied to the gate can control the polar state of a ferroelectric substrate. A  $180^\circ$  ferroelectric domain wall (**FDW**) in a ferroelectric substrate induces the formation of the p-n junction between the regions enriched with holes and electrons in graphene, which appear near the contact of the FDW with the surface of ferroelectric substrate [19, 20, 21]. The creation of p-n junctions in graphene have been realized earlier by doping of graphene channel by electrons or holes, respectively [22, 23, 24]. Then they have been studied theoretically [25, 26] and experimentally [27, 28, 29].

Notice, that p-n junctions can occur without any additional doping of graphene channel due to the charge separation by an electric field of FDWs near the surface [30, 31]. In general ballistic, diffusive and mixed types of carrier transport are possible in a graphene channel at a ferroelectric substrate with  $180^\circ$  FDWs [19, 20, 21]. It has been shown that the motion of FDWs in the substrate has a significant effect on the shape of current-voltage hysteresis loops of the GFET [19, 20, 21].

It is well-known that elastic strains can change the band structure of graphene and open its band gap [4, 5, 32, 33, 34]. One of the insufficiently investigated effects is the change of graphene conductivity due to the partial exfoliation of graphene from the ferroelectric substrate taking place when the voltage is applied to the gate of GFET, due to the presence of the piezoelectric effect in the substrate. Recently we have shown [35] that "up" and "down" vertical piezoelectric displacement of the ferroelectric domain surfaces can lead to the alternating stretching and exfoliation of graphene areas at the sections between elongated and contracted domains. Due to this, the conductance of graphene channel can be increased significantly at room temperature, because electrons in the clamped sections of graphene scatter mainly on ionized impurities in the ferroelectric substrate and intrinsic short-range imperfections in graphene, at the same time they

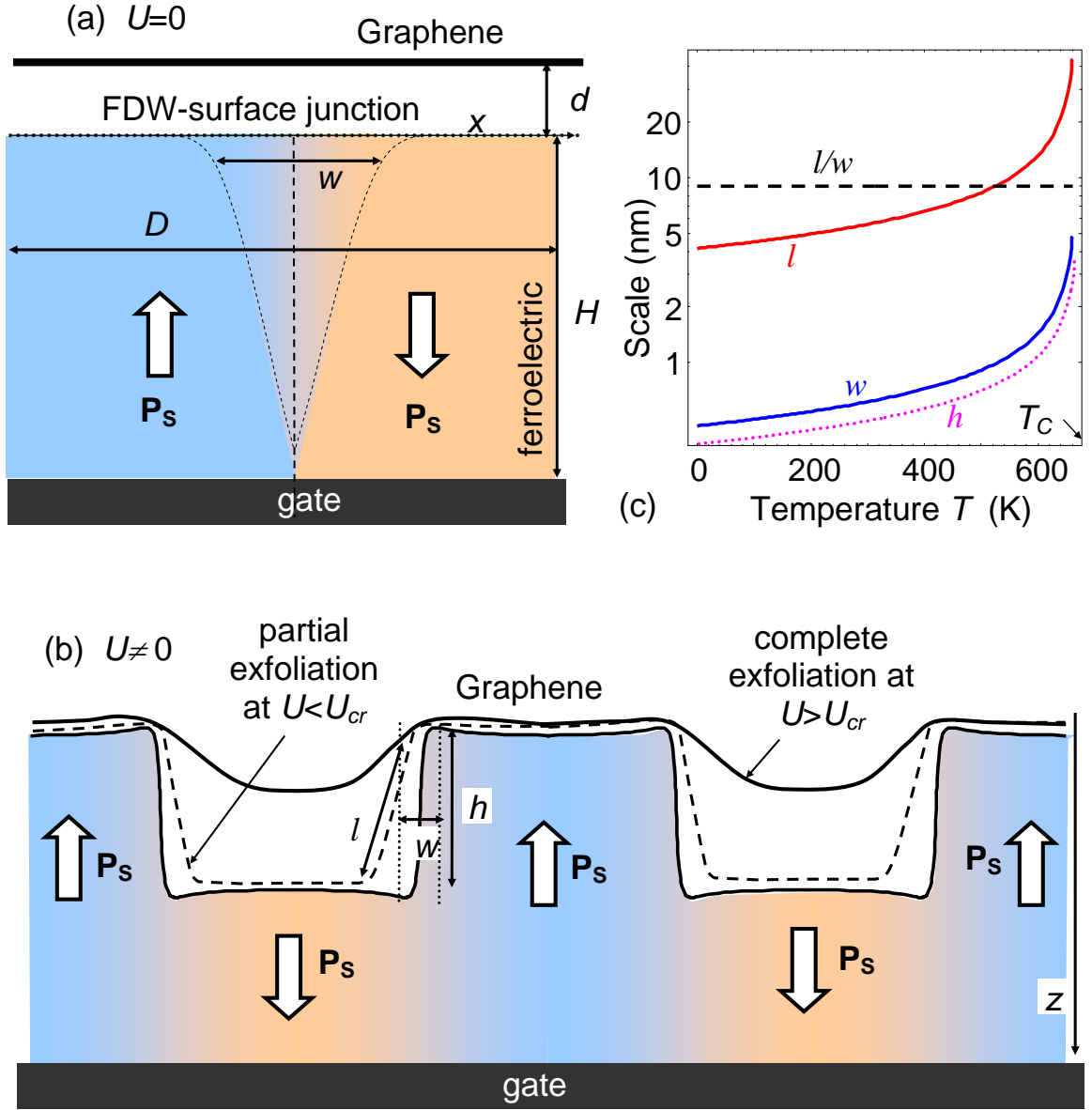
scatter on acoustic phonons in the stretched sections of graphene and the rate of this scattering channel is much lower.

Later we revealed a nontrivial temperature behavior of the carrier concentration in graphene that governs the conductance of the graphene channel on ferroelectric substrate with domain walls [36]. The effect originates from the nonlinear screening of ferroelectric polarization by graphene carriers, as well as it is conditioned by the temperature evolution of the domain structure kinetics in the ferroelectric substrate. The revealed piezoelectric mechanism of graphene conductance control requires systematic studies of the ambient condition impact on its manifestations.

To conclude we note that graphene and other 2D semiconductors on ferroelectric substrates are promising candidates for advanced field effect transistors, modulators and electrical transducers, providing that research of their electrical conductivity and electromechanical properties can be lifted up from ~~mostly~~ empirical to analytical level [37]. Therefore theoretical studies of the temperature behavior of the modulation of graphene channel conductance induced by piezoelectric effect in the ferroelectric substrate with domain walls are required. This theoretical work studies in details the nontrivial temperature behavior of the graphene conductance changes induced by piezoelectric effect in a ferroelectric substrate with domain structure.

## II. THEORETICAL BACKGROUND

Performed calculations [35] have shown that one ferroelectric domain elongates and another one contracts depending on the polarity of voltage  $U$  applied to a gate of the GFET on a ferroelectric substrate with FDW [compare **Fig. 1(a)** with **1(b)**]. The resulting displacement  $h$  of the ferroelectric surface can be significant and reach (0.5 – 1)nm for ferroelectric films with high piezoelectric coefficients like  $\text{PbZr}_{0.5}\text{Ti}_{0.5}\text{O}_3$  (**PZT**). The vertical scale in **Fig. 1(b)** is about (50 – 500) pm depending on the film thickness and temperature, while the horizontal scale is typically much larger and reaches (50 – 500) nm, or even microns (see e.g. **Fig.2** in Ref.[35]). The scales are so different because uncharged FDWs are usually thin (their thickness  $w$  is about (1 – 2) nm), and domain period is much longer (about 10 nm – 1  $\mu\text{m}$ ) depending on temperature and ferroelectric film thickness. The broadening of FDW appears near the free ferroelectric surface, at that the width of FDW increases in several times [see Ref.[38] and dashed curves in **Fig. 1(a)**].



**FIG. 1.** Partial exfoliation of graphene channel sections induced by a piezoelectric effect in the ferroelectric substrate with FDWs. The effect is absent at  $U=0$  (a) and appears at  $U\neq 0$  (b), when partial exfoliation [dashed curves in plot (b)] or complete exfoliation [solid curves in plot (b)] of graphene becomes possible. For complete exfoliation the maximal length of exfoliated regions is equal to the length of domains, which contract, i.e. the length  $l(T,U) < L/2$ . Dashed curves in plot (a) show the FDW broadening near the surface. (c) Dependence of the domain wall width  $w$  (blue curve) and exfoliated length  $l$  (red curve), their ratio  $l/w$  (black dashed line) and surface displacement  $h$  (magenta dotted curve) on temperature for graphene and PZT parameters, gate voltage  $U=1\text{V}$ ,  $d = 0.5 \text{ nm}$ ,  $H=1\mu\text{m}$  and binding energy  $J=0.25 \text{ J/m}^2$ .

When the voltage  $U$  is applied to a gate of the GFET with FDW, one domain elongates and another one contracts depending on the voltage polarity. Following Ref.[35], the surface displacement  $h$  depends on applied voltage  $U$  and temperature as

$$h = 2|U|[d_{33}(T) + (1 + 2\nu)d_{31}(T)] \approx \begin{cases} 2|U| \frac{d_{33}^0 + (1 + 2\nu)d_{31}^0}{\sqrt{1 - T/T_C}}, & T < T_C, \\ 0, & T > T_C. \end{cases} \quad (1)$$

Here  $\nu$  is the Poisson ratio [39]. Constants  $d_{33}$  and  $d_{31}$  are temperature-dependent piezoelectric coefficients,  $d_{33}(T) = \frac{d_{33}^0}{\sqrt{1 - T/T_C}}$  and  $d_{31}(T) = \frac{d_{31}^0}{\sqrt{1 - T/T_C}}$ , which increase when approaching Curie temperature and then becomes zero at  $T > T_C$  [40]. For PZT  $\nu=0.3$ ,  $d_{33}^0=741.316$  pm/V,  $d_{31}^0 = -333.592$  pm/V and  $T_C=666$  K [41].

Let us underline that approximate equality in Eq.(1) becomes invalid in the immediate vicinity of  $T_C$ , since  $h$  diverges as  $\frac{1}{\sqrt{1 - T/T_C}}$ , that is unphysical. Natural limitations imposed on the applicability of expression (1) for  $h$  value was discussed in Ref.[42]. This is the standard limitations of the linear decoupling approximation [43, 44, 45, 46] applicability for calculation of the elastic displacement of ferroelectric surface in response to applied electric voltage caused by piezoelectric effect. For a considered case the decoupling approximation is valid if  $h \ll H$ , where  $H$  is the thickness of ferroelectric film.

Below the ferroelectric film thickness is regarded thick enough ( $H=1 \mu\text{m}$ ) to satisfy the strict inequality  $h \ll H$  at all temperatures except for very thin immediate vicinity of  $T_C$ . Actually from **Fig.1(c)** the surface displacement  $h$  reaches 5 nm and higher when  $T$  approaching  $T_C$ . So that in accordance with the figure a minimum thickness threshold is about 50 nm, and below it the thickness  $H$  will critically affect on the calculated results validity. Note that the ferroelectric substrate was regarded thick enough ( $H= 1 \mu\text{m}$ ) to satisfy the inequality  $h \ll H$ . Actually from **Fig.1(c)** the surface displacement  $h$  reaches 5 nm and higher when  $T$  approaching  $T_C$ . So that in accordance with the inequality  $h \ll H$  a minimal thickness threshold is about  $H=50$  nm, and below it the thickness  $H$  will critically affect on the validity of analytical expressions derived below. However much more strict limitation on  $H$  follows from the fact that the Curie temperature  $T_{cr}(H)$  of the substrate can be tuned by changing its thickness  $H$  due to the finite size effects [47],

$T_{cr}(H) \approx T_C - \frac{d}{\alpha_T \varepsilon_0 \varepsilon_d H}$  [21, 31, 35]. The critical thickness of ferroelectricity disappearance

$H_{cr}(T) \approx \frac{d}{\alpha_T \varepsilon_0 \varepsilon_d (T_C - T)}$  can be estimated as (58 – 580) nm for the relative dielectric permittivity

of the physical gap  $\varepsilon_d = (1 - 10)$ , its thickness  $d=0.5$  nm, universal dielectric constant  $\varepsilon_0 = 8.85 \times 10^{-12}$  F/m,  $T=300$  K and PZT parameters, inverse Curie-Weiss constant  $\alpha_T = 2.66 \times 10^5 \text{ C}^{-1}$

$2 \cdot \text{mJ/K}$  and Curie temperature  $T_c=666 \text{ K}$ . From the above expressions  $T_{cr}(H)$  can be close to the room temperature for  $H \approx H_{cr}(T)$ .

The conductance of graphene channel in diffusion regime can change essentially, because electrons in the separated stretched section scatter on acoustic phonons, while more intensive scattering channel dominates in bounded sections [26]. In particular the voltage dependence of the graphene channel conductance  $G(T,U)$  corresponding to the case when its part of length  $l(U)$  is separated and another part of length  $L-l(U)$  is bounded, obeys the Matienssen rule [26]:

$$G(T,U) = \begin{cases} W \left( \frac{L-l(T,U)}{\sigma_B(T)} + \frac{l(T,U)}{\sigma_s(T)} \right)^{-1}, & L \geq 2l(T,U) \\ W \frac{L}{2} \left[ \frac{1}{\sigma_B(T)} + \frac{1}{\sigma_s(T)} \right]^{-1}, & L < 2l(T,U) \end{cases} \quad (2a)$$

Here  $L$  is graphene channel length and  $W$  is its width. All the temperature changes of graphene channel conductance (considered below) originates from the temperature changes of  $h$ , because

$l(T,U)$  is linearly proportional to  $h$ , namely  $l = h \cdot \sqrt[3]{\frac{Yd}{2J}}$  as it was derived in Ref.[35]. Regarding

that the factor  $\sqrt[3]{\frac{Yd}{2J}}$  is temperature independent, the expression for the temperature dependence of separated length  $l$  has the form

$$l(T,U) = \sqrt[3]{\frac{4Yd}{J}} [d_{33}(T) + (1+2\nu)d_{31}(T)] \cdot |U| \approx \begin{cases} \sqrt[3]{\frac{4Yd}{J}} \frac{(d_{33}^0 + (1+2\nu)d_{31}^0)}{\sqrt{1-T/T_c}} |U|, & T < T_c \\ 0, & T > T_c \end{cases} \quad (2b)$$

Here  $d$  is the distance between the flat surface of ferroelectric and graphene, and its thickness is determined by Van-der-Waals interaction being less than 1 nm. The density  $J$  of binding energy for graphene on ferroelectric should be smaller that the one for  $\text{SiO}_2$  substrate because graphene adhesion to mica surface is considered to be the strongest one in comparison with other surfaces ( $0.5 \text{ J/m}^2$ ) [48]. On the contrary the Young's modulus of graphene is extremely high ( $Y = 1 \text{ TPa}$  [49, 50]). Note that the linear approximation in Eq.(2a) of the separated graphene region,  $l(T,U) \sim |U|$ , can be used for the case when the length  $l$  is at least longer than the lateral halfwidth  $w/2$  of the ferroelectric surface displacement step at the FDW [see **Fig.1(b)**]. Since the width  $w$  is restricted by the intrinsic width of the uncharged domain wall that's temperature dependence is given by expression  $\sqrt{g/\alpha_T(T_c - T)} \sim w_0/\sqrt{1-T/T_c}$ , where  $w_0 = \sqrt{g/\alpha_T T_c}$  is the intrinsic width of uncharged domain wall at 0 K. The value  $w_0$  is about lattice constant ( $\sim 0.5 \text{ nm}$  in the bulk of

PZT). So that the ratio  $l(T,U)/w$  is temperature independent and equal to  $\sqrt[3]{\frac{4Yd}{J} \frac{|U|}{w_0} (d_{33}^0 + (1+2\nu)d_{31}^0)}$  in accordance with Eq.(2) and appeared about 10 for PZT parameters  $U=1$  V  $d = 0.5$  nm and  $J=0.25$  J/m [see **Fig.1(c)**].

The critical temperature corresponding to the condition  $2l(T_{cr},U) = L$  is given by expression

$$T_{cr}(L,U) = T_c \left[ 1 - \left( \frac{2|U|}{L} \cdot \sqrt[3]{\frac{4Yd}{J} (d_{33}^0 + (1+2\nu)d_{31}^0)} \right)^2 \right] \quad (3a)$$

At fixed temperature  $T < T_c$  the critical voltage corresponding to the condition  $2l(T,U_{cr}) = L$  is given by expression

$$|U_{cr}| = \sqrt[3]{\frac{J}{4Yd} \frac{\sqrt{1-T/T_c}}{d_{33}^0 + (1+2\nu)d_{31}^0} \frac{L}{2}}, \quad T < T_c. \quad (3b)$$

The critical temperature and gate voltage correspond to complete separation of graphene above the contracted domains [see solid curves in **Fig.1(b)**].

Notice that the contribution of the intrinsic width of FDW is not included in the analytical expressions (2)-(3), as well as it was not considered in earlier Refs.[35] and [42]. The FDW  $w=(1-5)$  nm according to the estimates shown in **Fig.1(c)**, and so the domain period (10 nm – 1  $\mu$ m) is much larger depending on temperature and ferroelectric film thickness. Since the linear approximation (2b) for the separated graphene region,  $l \sim |U|$ , can be used for the case when the length  $l$  is at least longer than the FDW halfwidth  $w/2$  [see **Fig.1(b)**], the minimal "threshold" voltage  $U_{th}$  required for graphene separation can be estimated from the equality  $l = w/2$ . In accordance with Eqs.(2b) and definition  $w = w_0/\sqrt{1-T/T_c}$ , the ratio  $l/w$  is temperature

independent and equal to  $\sqrt[3]{\frac{4Yd}{J} \frac{|U|}{w_0} (d_{33}^0 + (1+2\nu)d_{31}^0)}$ . Using the equality

$\sqrt[3]{\frac{4Yd}{J} \frac{|U_{th}|}{w_0} (d_{33}^0 + (1+2\nu)d_{31}^0)} = \frac{1}{2}$  it is possible to estimate the threshold voltage as

$|U_{th}| = \sqrt[3]{\frac{J}{4Yd} \frac{w_0}{2(d_{33}^0 + (1+2\nu)d_{31}^0)}}$ . Hence  $U_{th}$  is temperature independent and its value is rather

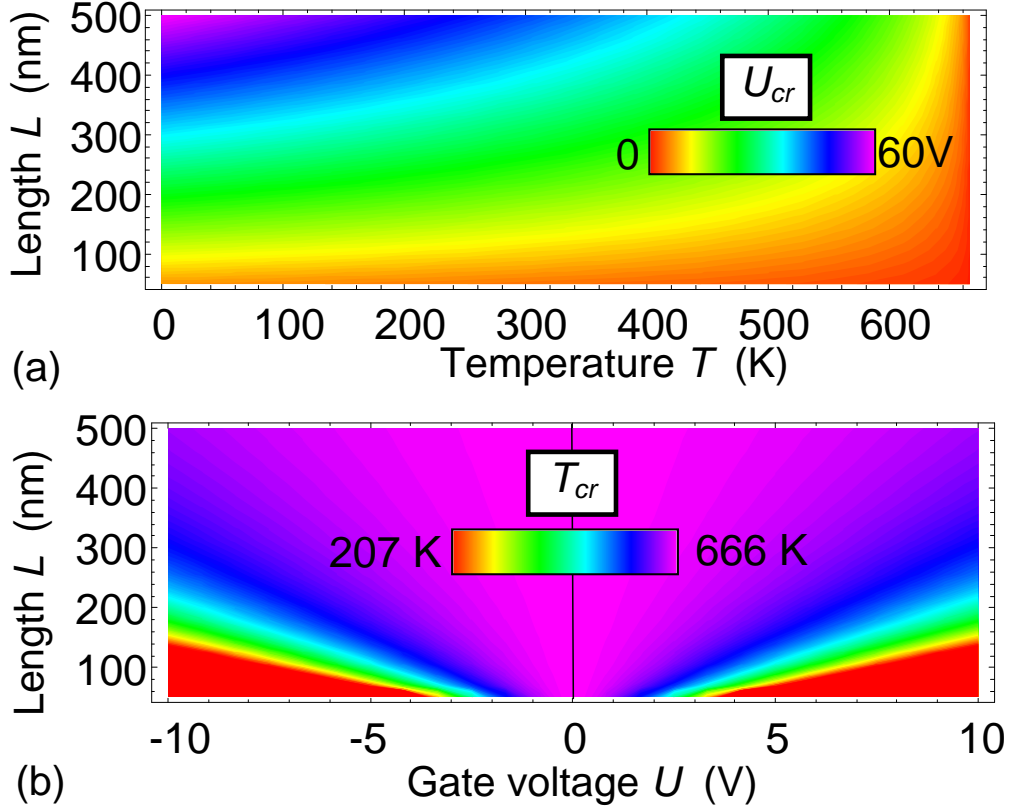
small, namely  $|U_{th}| = 0.06$  V for  $d = 0.5$  nm,  $J=0.25$  J/m<sup>2</sup> and PZT parameters.

### III. ANALYSIS OF THE CRITICAL GATE VOLTAGE AND TEMPERATURE

**Figure 2(a)** is the color map of the critical voltage  $U_{cr}(T, L)$  plotted in coordinates "temperature  $T$  – channel length  $L$ ". The value of  $U_{cr}$  varies from 0 at  $T = T_C$  to 60 V at  $T = 0$  K and  $L=500$  nm. At fixed  $L$  the value of  $U_{cr}$  monotonically increases with the temperature decrease, because  $|U_{cr}| \sim \sqrt{1-T/T_C}$  in accordance with Eq.(3b). At fixed  $T$  the value of  $U_{cr}$  linearly increases with  $L$  increase, because  $|U_{cr}| \sim L$  in accordance with Eq.(3b). **Fig. 2(a)** demonstrates the possibility to control graphene maximal separation by tuning the gate voltage  $U$  from 0 to  $U_{cr}$  for given temperature  $T$  and channel length  $L$ .

**Figure 2(b)** is the color map of the critical temperature  $T_{cr}(U, L)$  plotted in coordinates "gate voltage  $U$  – channel length  $L$ ". The value of  $T_{cr}$  varies from 207 K at  $U = \pm 10$  V and  $L=50$  nm to  $T_C=666$  K at  $U = 0$  and  $L=500$  nm. At fixed  $L$  the value of  $T_{cr}$  monotonically decreases with the gate voltage increase, because  $T_{cr}(L, U) = T_C \left[ 1 - \left( \frac{2|U|}{L} \cdot C \right)^2 \right]$  in accordance with Eq.(3a),  $C$  is a material constant. At fixed  $U$  the value of  $T_{cr}$  increases with  $L$  increase as  $1/L^2$  in accordance with Eq.(3a). **Figure 2(b)** demonstrates the possibility to control graphene maximal separation by tuning the ambient temperature  $T$  from 200 K to Curie temperature for a given gate voltage  $U$  and channel length  $L$ .





**FIG. 2.** (a) Color map of the critical voltage  $U_{cr}(T, L)$  plotted in coordinates "temperature  $T$  – channel length  $L$ ". (b) Color map of the critical temperature  $T_{cr}(U, L)$  plotted in coordinates "gate voltage  $U$  – channel length  $L$ ". Piezoelectric coefficients  $d_{33}^0=741.316$  pm/V,  $d_{31}^0=-333.592$  pm/V, Curie temperature  $T_C=666$  K and Poisson ratio  $\nu=0.3$  corresponds to  $\text{PbZr}_{0.5}\text{Ti}_{0.5}\text{O}_3$ . Graphene-ferroelectric separation  $d=0.5$  nm, binding energy  $J=0.25$  J/m<sup>2</sup> and graphene Young's modulus  $Y=1$  TPa. Color scale ranges from minimal (red color) to maximal (violet color) values indicated by numbers.

#### IV. TEMPERATURE AND LENGTH BEHAVIOR OF GRAPHENE CHANNEL CONDUCTANCE

The conductivity of the bounded section  $\sigma_B$ , where the scattering of electrons at substrate ionized impurities dominate, has the form listed in Refs.[3, 35]. Corresponding temperature dependence  $\sigma_B(T)$  has the form:

$$\sigma_B(T) = \frac{2e^2}{\pi^{3/2}\eta} \lambda_B[n_S(T)] \sqrt{n_S(T)} \approx \frac{2e\lambda_{B0}\sqrt{n_{S0}}}{\pi^{3/2}\eta} \sqrt{1 - \frac{T}{T_C}}, \quad T < T_C. \quad (4)$$

Here  $e=1.6 \times 10^{-19}$  C is elementary charge,  $\eta=1.056 \times 10^{-34}$  J·s =  $6.583 \times 10^{-16}$  eV·s is Plank constant,  $v_F=10^6$  m/s is characteristic electron velocity in graphene,  $\lambda_B[n_S]=\xi\sqrt{n_S}$  is mean free path in

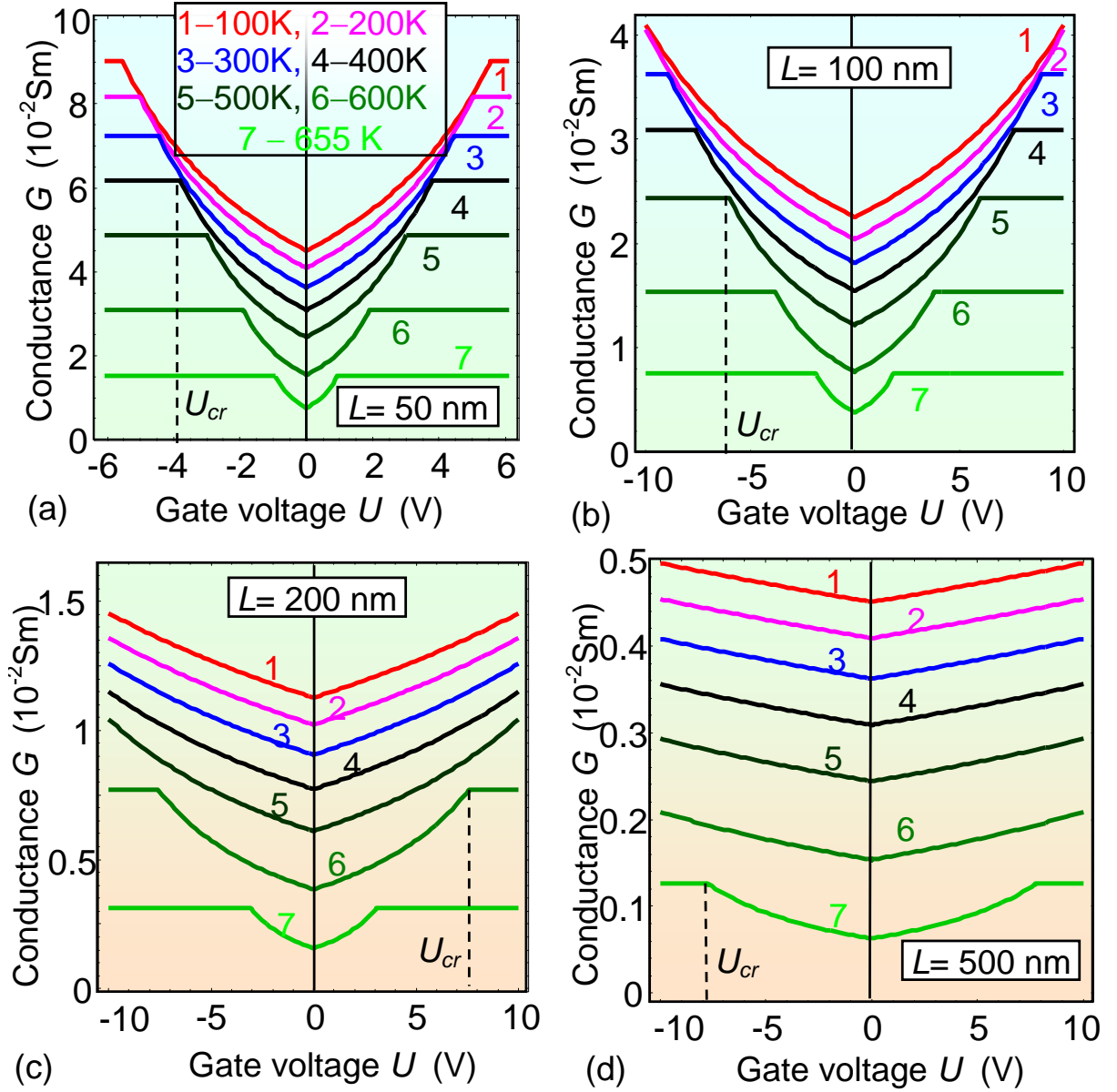
bounded graphene channel where scattering at ionized substrate impurities dominate [3] and the proportionality coefficient  $\xi$  depends on the substrate material and graphene-ferroelectric interface chemistry [26]. In Eq.(4) we assumed that the concentration  $n_s$  of 2D electrons can be regarded voltage-independent value far from the FDWs and proportional to the spontaneous polarization,  $P_s(T)$ , namely  $n_s(T) \approx |P_s(T)/e|$ . Because the temperature dependence of spontaneous polarization is  $P_s(T) = P_s^0 \sqrt{1 - \frac{T}{T_C}}$  we derived that  $n_s(T) \approx n_{s0} \sqrt{1 - \frac{T}{T_C}}$  and  $\lambda_B[n_s] = \lambda_{B0} \sqrt{1 - \frac{T}{T_C}}$ . Substitution of the latter expression in Eq.(4) gives the temperature dependence in the equation.

Conductivity of the separated stretched section of structurally perfect graphene is ruled by collisions with acoustic phonons  $\sigma_s$  and doesn't depend on 2D electrons concentration in the graphene channel. (see e.g. Refs.[21] and [35]). The upper limit for  $\sigma_s$  is:

$$\sigma_s(T) = \frac{4e^2 \eta \rho_m v_F^2 v_s^2}{\pi D_A^2 k_B T} \quad (5)$$

In Eq.(5)  $\rho_m \approx 7.6 \cdot 10^{-7} \text{ kg/m}^2$  is 2D mass density of carriers in graphene,  $v_s \approx 2.1 \cdot 10^4 \text{ m/s}$  is a sound velocity in graphene, Boltzmann constant  $k_B = 1.38 \times 10^{-23} \text{ J/K}$ ,  $D_A \approx 19 \text{ eV}$  is acoustic deformation potential that describes electron-phonon interaction [35].

**Figures 3(a-d)** illustrate the dependences of the conductance  $G(U, T)$  on the gate voltage  $U$  calculated for several temperatures  $T$  in the range (100 - 655) K and channel lengths  $L$  in the range (50 – 500) nm. From the figures the conductance, being a monotonically increasing function of  $|U|$  in accordance with Eqs.(2), becomes voltage independent at  $|U| > |U_{cr}|$ . At that the U-type curves of  $G(U, T)$  are the highest for the lowest temperature 100 K and monotonically sink down with the temperature increase to 655 K (compare the curves 1 – 7). The conductance decrease is more than 5 times with the temperature change from 100 K to 655 K. In accordance with Eq.(3b) and **Fig.2(a)** the value of  $|U_{cr}|$  increases with  $L$  increase from 1 V to 10 V and higher. Because of the fact the voltage region of U-type curves of  $G(U, T)$  significantly increases with  $L$  increase from 50 nm to 500 nm [compare plots (a) – (d)].



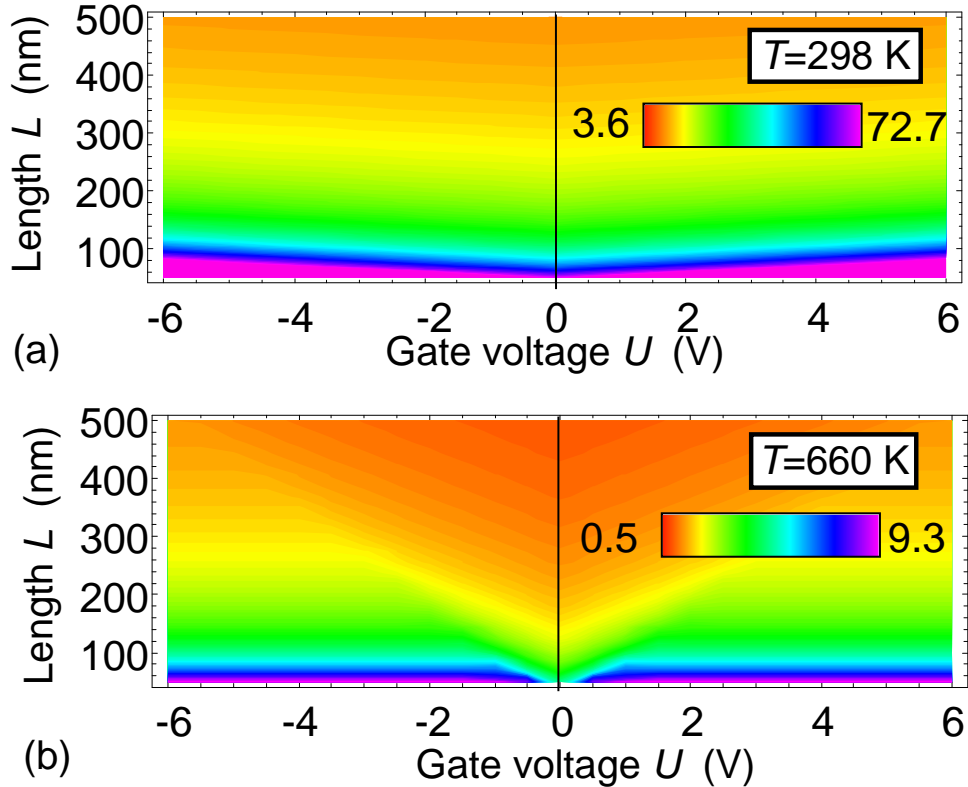
**FIG. 3.** Dependences of the conductance  $G(U, T)$  on the gate voltage  $U$  calculated for several temperatures  $T=100, 200, 300, 400, 500, 600$  and  $655 \text{ K}$  (curves 1 – 7) and channel length  $L = 50 \text{ nm}$ , (a)  $100 \text{ nm}$  (b),  $200 \text{ nm}$  (c),  $500 \text{ nm}$  (d). Electron mean free path  $\lambda_{B0} = 10 \text{ nm}$  and concentration  $n_{S0} = 3 \times 10^{18} \text{ m}^{-2}$  at  $T = 0$ , channel width  $W = 50 \text{ nm}$ . Other parameters are the same as in **Fig. 2**.

In this way **Figs 3** quantify the impact of piezoelectric effect on the voltage dependence of graphene channel conductance. Actually, by tuning the gate voltage  $U$  from 0 to  $U_{cr}$  at *different* temperatures ( $T$  is different for each of the curves 1 - 7) and *fixed* channel length ( $L$  is different for each of the plots (a)-(d)) one can change  $G(U)$  value in several times (from 2 to 8).

**Figure 4(a)** is the color map of the graphene channel conductance  $G(T, U)$  plotted in coordinates "gate voltage  $U$  – channel length  $L$ " calculated at room temperature. The value of  $G(T, U)$  varies from  $3.6 \text{ mSm}$  for  $U=0$  and  $L=500 \text{ nm}$  to  $72.7 \text{ mSm}$  for  $|U|=6 \text{ V}$  and  $L=50 \text{ nm}$ . At

fixed  $L$  the value of  $G(T,U)$  relatively slowly and quasi-linearly increases with the  $U$  increase until  $|U| < |U_{cr}(L,T)|$ , where  $|U_{cr}(L,T)|$  follows from Eq.(3b). At fixed gate voltage  $|U| < |U_{cr}(L,T)|$  the value of  $G(T,U)$  significantly decreases with  $L$  increase, because the ratio  $l/L$  decreases in accordance with Eq.(1).

**Figure 4(b)** is color map of the conductance  $G(T,U)$  plotted in coordinates "gate voltage  $U$  – channel length  $L$ " calculated at temperature 660 K that is very close to  $T_C$ . The value of  $G(T,U)$  varies from 0.5 mSm for  $U=0$  and  $L=500$  nm to 9.3 mSm for  $|U|=6$  V and  $L=50$  nm. At fixed  $L$  the value of  $G(T,U)$  noticeably quasi-linearly increases with the  $U$  increase until  $|U| < |U_{cr}(L,T)|$ , where  $|U_{cr}(L,T)|$  follows from Eq.(3b). At fixed gate voltage  $|U| < |U_{cr}(L,T)|$  the value of  $G(T,U)$  significantly decreases with  $L$  increase, because the ratio  $l/L$  decreases in accordance with Eq.(1). Despite the color map 4(b) demonstrates significant changes with  $U$  increase, and the absolute values of the conductance at 660 K are much lower than the ones at room temperature.



**FIG. 4.** Color maps of the conductance  $G(T,U)$  (in mSm) plotted in coordinates "gate voltage  $U$  – channel length  $L$ " calculated at room temperature 298 K (a) and 660 K (b). Other parameters are the same as in Fig. 2. Color scale ranges from minimal (red color) to maximal (violet color) values indicated by numbers.

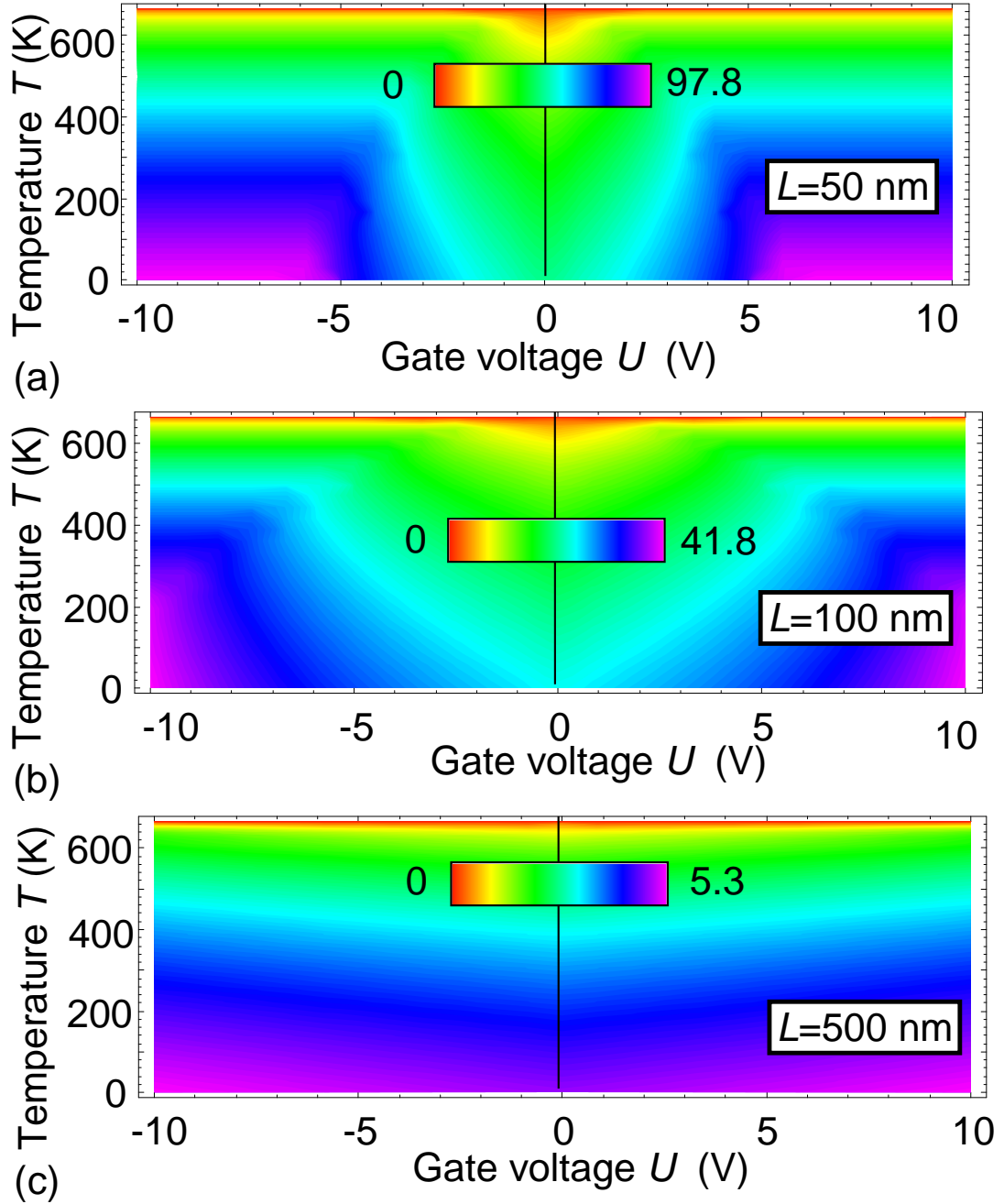
**Figure 5(a)** is the color map of the graphene channel conductance  $G(T,U)$  plotted in coordinates "gate voltage  $U$  – temperature  $T$ " calculated for  $L=50$  nm. The value of  $G(T,U)$  varies from 0 for  $T=T_C$  to 97.8 mSm for  $|U|=10$ V and  $L=50$  nm. At fixed  $T$  the value of  $G(T,U)$  increases in a quasi-parabolic way with  $U$  increasing until  $|U| < |U_{cr}(L,T)|$ , where  $|U_{cr}(L,T)|$  follows from Eq.(3b). At fixed gate voltage  $|U| < |U_{cr}(L,T)|$  the value of  $G(T,U)$  significantly decreases with  $T$  increase, because the ratio  $l/L$  decreases in accordance with Eq.(1).

**Figure 5(b)** is color map of the conductance  $G(T,U)$  plotted in coordinates "gate voltage  $U$  – temperature  $T$ " calculated for  $L=100$  nm. The value of  $G(T,U)$  varies from 0 for  $T=T_C$  to 41.8 mSm for  $|U|=10$ V and  $L=100$  nm. At fixed  $T$  the value of  $G(T,U)$  noticeably increases with the  $U$  increase until  $|U| < |U_{cr}(L,T)|$ .

**Figure 5(c)** is color map of the conductance  $G(T,U)$  plotted in coordinates "gate voltage  $U$  – temperature  $T$ " calculated for  $L=500$  nm.. The value of  $G(T,U)$  varies from 0 for  $T=T_C$  to 5.3 mSm for  $|U|=10$ V and  $L=500$  nm. At fixed  $T$  the value of  $G(T,U)$  slightly quasi-linearly increases with the  $U$  increase, the critical voltage is high and not shown in the figure.

To resume numerical results performed for graphene on PZT ferroelectric substrate and shown in **Figs.2-5**, we note that graphene channel conductance can be changed in 5-100 times by changing the temperature from low values to either the critical value  $T_{cr}$  or to ferroelectric Curie temperature (666 K for PZT) depending on the gate voltage  $U$  and channel length  $L$ . Also we demonstrate the possibility to change graphene conductance up to 100 times by tuning voltage  $U$  from 0 to the critical value  $U_{cr} \sim (1 - 10)$  V at a given  $T$  and  $L$ . Thus color maps, shown in **Figs. 4** and **5**, demonstrate that it is possible to control graphene channel conductance  $G(U)$  in a wide range by changing the temperature  $T$  or channel length  $L$ .

All above numerical results were performed for a thick PZT substrate with relatively high  $T_C = 666$  K. Another ferroelectric material can be chosen as substrate with e.g. lower Curie temperature, such as BaTiO<sub>3</sub> with  $T_C = 381$  K.



**FIG. 5.** Color maps of the conductance  $G(T, U)$  (in mSm) plotted in coordinates "gate voltage  $U$  – temperature  $T$ " calculated for several channel length  $L= 50$  nm (a) 100 nm (b) and 500 nm (c). Other parameters are the same as in Fig. 2. Color scale ranges from minimal (red color) to maximal (violet color) values indicated by numbers.

## V. DISCUSSION AND CONCLUSIONS

This work demonstrates the possibility of increasing up to 100 times the conductance of graphene channel on a ferroelectric substrate with  $180^\circ$  domain walls by changing ambient temperature  $T$  from low values to the critical one  $T_{cr}$  for a given gate voltage  $U$  and channel length  $L$ . For a graphene on PZT substrate with  $180^\circ$  domain walls we revealed the possibility to change

the graphene conductance up to 100 times by increasing  $U$  from 0 to the critical value  $U_{cr}$  at a given  $T$  and  $L$ . The critical parameters  $T_{cr}$  and  $U_{cr}$  correspond to complete exfoliation of graphene sections above contracted domains. We derived analytical expressions for the dependence of the critical voltage  $U_{cr}$  and graphene conductance  $G(U)$  on  $T$ ,  $L$  and material parameters of graphene-on-ferroelectric structure.

Obtained results require urgent experimental verification, since they can open the way towards advanced applications of graphene on ferroelectric in piezo-resistive memories operating in a wide temperature range. Discussing the possibilities of experimental verification of our theoretical predictions, we should discuss a number of limitations on their applicability. In particular, presented theoretical results are obtained in a thermodynamic limit. Realistic operation speed of GFET and its physical limitations are very important for practical applications. The time required for the piezoelectric displacement of ferroelectric domains induced by electric voltage—is defined by the Khalatnikov relaxation time,  $\tau_K$  [35]. The time  $\tau_K$  varies in the range  $(10^{-11} - 10^{-13})$ s typical for acoustic phonons relaxation far from  $T_C$  [21, 36, 46]. On this basis, the operating frequency  $f$  and acoustic wave velocity  $w$  can be estimated as  $f = \tau_K^{-1} = (0.1 - 10)$  THz and  $V = h/\tau_K = (10^2 - 10^4)$ m/s, respectively. The Khalatnikov coefficient  $\Gamma$  in the time-dependent Landau-Ginzburg-Devonshire (**LGD**) equation for ferroelectric polarization determines the relaxation time  $\tau_K$  in accordance with expression  $\tau_K = \Gamma/|\alpha_T(T - T_C)|$  [46]. However  $\tau_K$  determines the lower limit of the operating time for GFET device, because the real time of the domain wall motion can be affected by lattice pinning barriers and defects [46]. Pinning can increase the time of the domain wall motion in 1-2 orders of magnitude higher than  $\tau_K$  and thus decrease the frequency  $f$  to 1 GHz – 1 THz.

Going beyond the scope of thermodynamic limit, the dynamic piezoelectric hysteresis effect can occur. Actually, piezo-hysteresis effect will be observed when the gate voltage  $U(t)$  varies periodically with time, because different physical mechanisms are responsible for direct increase and converse decrease of exfoliated and clamped channel sections lengths during the cycling of gate voltage. The question is whether the thermodynamic LGD— approach, that we used for a ferroelectric substrate description, is applicable to describe quantitatively all important characteristics of the hysteresis effect, or its application is relevant for the description of some of them only. In principle thermodynamic LGD approach estimates correctly the temperature dependence of the remanent spontaneous polarization, width and period of FDWs, as well as the temperature hysteresis of these values inherent to the ferroelectrics and their thin films with the first order phase transition to a paraelectric phase [47, 51]. However LGD approach typically overestimates (sometimes in 10 – 100 times) the value of coercive field, since the continual

approach does not account for creep and pinning of FDWs by lattice barriers and defects [52, 51, 53, 54]. Complementary methods (such as discrete models, *ab initio* calculations, etc) should be used for the coercive field calculations. Taking into account the above argumentation, we cannot apply the obtained results for quantitative description of piezo-hysteresis effect, but can forecast the possibility of its observation in GFETs. Finally, we should mention that there are exciting possibilities to realize the dynamical piezo-hysteresis effect in practice and its characteristics should significantly depend on the GFET operating frequency.

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